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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TAKEGUCHI, KATHY K

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2187	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/607,300	Applicant(s) WEBER ET AL.	
	Examiner Kathy Takeguchi	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is a Non-Final Action taken in response to examination of Claims 1-10 and 12-23, presented in the application. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

Claim Objections

2. Claims 3-4, 6, and 19 are objected to because of the following informality:

In Claim 3, all citations of "back-end controllers" (e.g., line 4, line 5, and etc) should be changed to "back-end control elements" to be consistent with the previous citations.

In Claim 4, all citations of "back-end controllers" (e.g., line 8, line 10, and etc) should be changed to "back-end control elements" to be consistent with the previous citations.

In Claim 6, all citations of "back-end controllers" (e.g., line 22, line 23, line 25, line 26, and etc) should be changed to "back-end control elements" to be consistent with the previous citations.

In Claim 19 (page 5, line 28), "**and configured,.**" should be deleted from the sentence. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. The term "substantially" in claims 1, 14, and 19 is a relative term, which renders the claims indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Claims 2-13, 15-18, and 20-23 are rejected because they incorporate the indefiniteness of Claims 1, 14, and 19.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5-6, 13-14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi (United States Patent 5,396,596) in view of Liebhart et al ("A Study of an SCI Switch Fabric". IEEE. Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. Authors: Liebhart, Brenner, and Bogaerts. Pages162-169.).

As per Claim 1:

Hashemi teaches a storage system comprising:

- a plurality of front-end control elements devoid of circuits and functions that control a plurality of I/O devices and configured for controlling information exchange using RAID storage management with one or more attached host computer systems (e.g., CIM: Channel Interface Module, element 8c in Figures 1A and 1B)

- a plurality of back-end control elements devoid of circuits and functions that interface directly with the attached host computer systems, communicatively coupled to a plurality of I/O devices and configured for controlling information exchange with the I/O devices (e.g., DIM: Device Interface Module, element 8d in Figures 1A and 1B)

- wherein the front-end control elements differ in number from the back-end control elements (e.g., Column 2, lines 53-57: "Various functional control module rack (CMR) configurations permit ***any combination of Channel Interface Modules (CIM) and Device Interface Modules (DIM)***, configured up to a maximum of 8 separate modules"; Figure 1A: Note box labeled "CIM **or** DIM")

- and an interconnect element coupled to said front-end control elements and coupled to said back-end control elements to enable exchange of information therebetween, wherein the storage system is adapted to implement additional front-end control elements, back-end control elements and interconnect elements independent of all other such elements,

wherein the interconnect element is configured for conveying the requests from the front-end control elements to the back-end control elements to perform the host requested I/O operation (e.g., Column 3, line 55 to Column 4, line 31).

Hashemi does not specifically disclose the interconnect element as being a SAN architecture fabric. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

However, Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as a SAN interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI switch fabric is a high speed interconnect system, designed and specified as a topology independent protocol (i.e., interfacable to PCI, VME, *Futurebus*, ATM, Fibre Channel, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

Hashemi's system provides limited scalability in that it is configurable "up to a maximum of 8 separate modules" (e.g., Column 2, lines 53-57). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Liebhart

with Hashemi for the desirable purpose of system scalability and expansion as well as for providing a high speed, topology independent protocol.

As per Claim 2:

Hashemi further teaches a plurality of disk drives coupled as I/O devices to said back-end control elements (e.g., element 70 in Figures 1A and 1B).

As per Claim 3:

Hashemi teaches a plurality of disk drives comprising:

- a first subset of said plurality of disk drives (e.g., 70a and 70b in Figure 1A);
- a second subset of said plurality of disk drives (e.g., 70c and 70d in Figure 1A);
- wherein said plurality of back-end control elements includes:
    - o a first pair of back-end control elements (e.g., 8d1 and 8d2 in Figure 1A) coupled to said first subset; and
    - o a second pair of back-end control elements (e.g., 8d1 and 8d2 in Figure 1A) coupled to said second subset.

Note: The limitations in the claim do not specify that the first pair of back-end control elements is different than the second pair of back-end control elements.

As per Claim 5:

Hashemi further teaches a system, wherein the interconnect element comprises a pair of interconnect elements (e.g., element 6a and element 6b in Figure 1A) and wherein each of said plurality of front-end control elements is coupled to each of said pair of interconnect elements (e.g., Figure 1A).

As per Claim 6:

Hashemi teaches a system further comprising:

- a first set of disk drives (e.g., 70a and 70b in Figure 1A);
- a second set of disk drives (e.g., 70c and 70d in Figure 1A) and wherein said plurality of back-end control elements including:
    - a first pair of back-end elements (e.g., 8d1 and 8d2 in Figure 1A) coupled to said first set, wherein each of said first pair of back-end elements is coupled to a corresponding one of said pair of interconnect elements (e.g., either 70a or 70b in Figure 1A);
    - and a second pair of back-end controllers (e.g., 8d1 and 8d2 in Figure 1A) coupled to said second set wherein each of said second pair of back-end elements is coupled to a corresponding one of said pair of interconnect elements (e.g., either 70a or 70b in Figure 1A).

As per Claim 13:

Hashemi further teaches that his system can be configurable to support a RAID technology in either RAID 0, RAID 3, or RAID 5 (e.g., Column 2, lines 64-68). RAID 3 and RAID 5 both utilize a parity assist element for RAID parity generation and checking.

As per Claim 14:

Hashemi teaches a front-end control element for a storage subsystem comprising:

- a host system interface (e.g., elements labeled as I1 and I2 in element 8c in Figure 1A); and
- a processor coupled to said host system interface to process host system generated I/O requests received through said host system interface (e.g., host processors labeled as 4a, 4b, 4c, and 4d in Figure 1A).

Hashemi also teaches an interface coupled to said processor for coupling said front-end control element to a plurality of back-end control elements (e.g., FB1 and FB2 in Figure 1A; Column 9, lines 58-65: "any channel interface module (CIM) can talk to any one of the device interface modules thru the Futurebus state machines).

Additionally, Hashemi teaches a system, wherein the front-end control element (e.g., CIM) is adapted to be added to the storage subsystem independent of said back-end control elements, wherein front-end control elements differ in number from said back-end control elements (e.g., Column 2, lines 53-57: "Various functional control module rack (CMR) configurations permit

any combination of Channel Interface Modules (CIM) and Device Interface Modules (DIM), configured up to a maximum of 8 separate modules"; Figure 1A: Note box labeled "CIM **or** DIM").

Furthermore, Hashemi teaches an interconnect between the front-end control elements and the back-end control elements allowing for the conveying of I/O requests from the front-end control elements to the back-end control elements by the exchange of messages between the front-end and back-end control elements according to address indicia within the messages and associated with the front-end and back-end control elements. Also, Hashemi teaches a system, wherein the front-end control element is devoid of circuits and functions that control a plurality of I/O devices.

Hashemi does not specifically disclose the interconnect element as being a SAN architecture fabric. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

However, Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as an interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI switch fabric is a high speed interconnect system, designed and specified as a topology independent protocol (i.e., interfacable to PCI, VME, *Futurebus*, ATM, Fibre Channel, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a

coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

Hashemi's system provides limited scalability in that it is configurable "up to a maximum of 8 separate modules" (e.g., Column 2, lines 53-57). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Liebhart with Hashemi for the desirable purpose of system scalability and expansion as well as for providing a high speed, topology independent protocol.

As per Claim 19:

Hashemi teaches a back-end control element for a storage subsystem comprising:

- a disk drive interface for coupling said back-end control element to a plurality of disk drives (e.g., elements labeled as D1 in element 8d in Figure 1A).

Hashemi also teaches an interface coupled to said processor for coupling said front-end control element to a plurality of back-end control elements (e.g., Column 9, lines 58-65: "any channel interface module (CIM) can talk to any one of the device interface modules thru the Futurebus state machines).

Additionally, Hashemi teaches a system, wherein the front-end control element (e.g., CIM) is adapted to be added to the storage subsystem independent of said back-end control elements,

wherein front-end control elements differ in number from said back-end control elements (e.g., Column 2, lines 53-57: "Various functional control module rack (CMR) configurations permit ***any combination of Channel Interface Modules (CIM) and Device Interface Modules (DIM)***, configured up to a maximum of 8 separate modules"; Figure 1A: Note box labeled "CIM **or** DIM").

Furthermore, Hashemi teaches an interconnect between the front-end control elements and the back-end control elements allowing for the conveying of I/O requests from the front-end control elements to the back-end control elements by the exchange of messages between the front-end and back-end control elements according to address indicia within the messages and associated with the front-end and back-end control elements. Also, Hashemi teaches a system, wherein the back-end control element is devoid of circuits and functions that interface directly with the attached host computer systems.

Hashemi does not specifically disclose the interconnect element as being a SAN architecture fabric. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

However, Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as an interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI switch fabric is a high speed interconnect system, designed and specified as a topology

independent protocol (i.e., interfacable to PCI, VME, *Futurebus*, ATM, Fibre Channel, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

Hashemi's system provides limited scalability in that it is configurable "up to a maximum of 8 separate modules" (e.g., Column 2, lines 53-57). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Liebhart with Hashemi for the desirable purpose of system scalability and expansion.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi (United States Patent 5,396,596) in view of Liebhart et al ("A Study of an SCI Switch Fabric". IEEE. Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. Authors: Liebhart, Brenner, and Bogaerts. Pages162-169.) and in further view of Otteson et al (United States Patent 6,571,310).

As per Claim 4:

Hashemi and Liebhart teach the system disclosed in Claims 1-3, but do not specifically disclose redundant links coupling the back-end control elements to a set of disk drives.

However, Otteson discloses a storage system including a storage controller and plurality of disk drives. Otteson specifically discloses that various configurations are possible and that "disk drives may be attached to redundant buses, bus interfaces, storage controllers, and other elements" (e.g., Column 8, lines 35-46). Furthermore, Otteson discloses that the inclusion of such elements such as redundant buses coupling the controller to the disk drives would provide the added feature of ensuring "that no failure of any single component will cause data to be inaccessible" (e.g., Column 8, lines 35-46).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Otteson with Hashemi and Liebert because an extra bus would allow for an alternate connection to the disk drive.

8. Claims 8, 16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi (United States Patent 5,396,596) in view of Liebhart et al ("A Study of an SCI Switch Fabric". IEEE. Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. Authors: Liebhart, Brenner, and Bogaerts. Pages162-169.) and in further view of Brown et al (United States Patent 6,148,414).

As per Claims 8, 16, and 21:

Hashemi does not specifically disclose the interconnect element as being a SAN architecture fabric. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as an interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI switch fabric is a high speed interconnect system, designed and specified as a topology independent protocol (i.e., interfacable to PCI, VME, *Futurebus*, ATM, *Fibre Channel*, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

However, Brown discloses that using a fiber-channel based SAN switch fabric is preferable as an interconnect medium because "the fiber-channel standard is an open standard that supports several network topologies including point-to-point, switched fabric, arbitrated loop, and any combination of these topologies" (e.g., Column 6, lines 24-43). Furthermore, fiber channel provides for the support of a number of protocols such as SCSI, Asynchronous Transfer Mode (ATM), Transmission Control Protocol/Internet Protocol (TCP/IP), and High Performance Parallel Interface (HiPPI), while also providing data transfer speeds of up to 100MBps.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brown with Hashemi and Liebhart for the purpose of having a communication medium with an open standard that supports several network topologies and protocols, while providing data transfer speeds of up to 100MBps.

9. Claims 7, 15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi (United States Patent 5,396,596) in view of Liebhart et al ("A Study of an SCI Switch Fabric". IEEE. Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. Authors: Liebhart, Brenner, and Bogaerts. Pages162-169.) and in further view of Hennessy et al (Computer Architecture: A Quantitative Approach. Morgan Kaufmann Publishers, Inc. Second Edition, 1996. Page 573.).

As per Claims 7, 15 and 20:

Hashemi does not specifically disclose the interconnect element as being a SAN architecture fabric. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as an interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI

switch fabric is a high speed interconnect system, designed and specified as a topology independent protocol (i.e., interfacable to *PCI*, VME, *Futurebus*, ATM, Fibre Channel, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

However, the PCI bus is often used for fast I/O devices (Hennessy and Patterson, page 573) as in the system described within the claims. Additionally, it is known in the art that the use of PCI buses is prevalent in I/O architectures.

Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to specify a PCI bus as the interconnect for the purpose of providing a prevalent communication medium for fast I/O devices.

10. Claims 9-10, 17-18, and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi (United States Patent 5,396,596) in view of Liebhart et al ("A Study of an SCI Switch Fabric". IEEE. Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. Authors: Liebhart, Brenner, and Bogaerts. Pages 162-169.).

As per Claims 9, 17 and 22:

Hashemi does not specifically disclose the interconnect element as being an Infiniband compliant communication medium. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as an interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI switch fabric is a high speed interconnect system, designed and specified as a topology independent protocol (i.e., interfacable to PCI, VME, *Futurebus*, ATM, *Fibre Channel*, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

However, Infiniband provides for the serial transmission of data (e.g., as opposed to PCI, which has parallel transmission) to devices and is capable of carrying multiple channels of data at the same time in a multiplexing signal.

Thus, it would it would have been obvious at the time the invention was made to a person having ordinary skill in the art to specify the use of Infiniband as the communication medium because Infiniband would provide for the serial transmission of data (e.g., as opposed to PCI, which has

parallel transmission) to devices and is capable of carrying multiple channels of data at the same time in a multiplexing signal.

As per Claims 10, 18, and 23:

Hashemi does not specifically disclose the interconnect element as being a local area network communication medium. Instead, Hashemi teaches the use of *Futurebus*, "the industry standard", as the interconnect allowing for communication between CIM and DIM modules.

Liebhart teaches the concept of using the Scalable Coherent Interface (SCI) switch fabric as an interconnect system, allowing for communication across multiple nodes (e.g., Abstract). Liebhart teaches the SCI switch fabric as providing many advantageous features. The SCI switch fabric is a high speed interconnect system, designed and specified as a topology independent protocol (i.e., interfacable to PCI, VME, *Futurebus*, ATM, *Fibre Channel*, etc.). Additionally, Liebhart teaches the SCI switch fabric as being a scalable system allowing for a coherent memory system. Furthermore, the SCI switch fabric can convey the requests from the modules by the exchange of messages according to address indicia within the messages and associated with the modules.

However, local area network communication mediums are known for providing privately owned networks within a relatively small area (e.g., a few kilometers in size), while allowing various topology configurations.

Thus, it would it would have been obvious at the time the invention was made to a person having ordinary skill in the art to specify the use of a local area network communication medium for the purpose of taking advantage of a LAN's size, transmission technology, and topology.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi (United States Patent 5,396,596) in view of Liebhart et al ("A Study of an SCI Switch Fabric". IEEE. Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, 1997. Authors: Liebhart, Brenner, and Bogaerts. Pages162-169.) and in further view of Belsan et al (United States Patent 5,394,532).

As per Claim 12:

Hashemi and Liebert do not specifically mention that the front-end control is operable to perform the mapping of logical store addresses to physical store addresses for further operations by said back-end control element.

Belsan, however, teaches a control unit connected to both hosts and I/O devices. Belsan's control unit labeled as 101 in Figure 2 is operable to perform the major data storage control functions, which includes the mapping of logical storage addresses to physical storage addresses (e.g., Column 5, lines 8-16; Column 7, lines 36-53; Column 8, lines 47-52). Belsan teaches that the mapping of logical to physical storage addresses provides for identifying the exact physical location of the particular disk drive that contains data identified by the host processor.

Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have a control unit with the ability to map logical storage addresses to physical storage addresses because logical addresses do not relate directly to a physical location and need to be translated or mapped to physical addresses in order to obtain the actual physical location. Hence, a controller usually performs a logical to physical address conversion to be able to access the data from the exact physical location.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kathy Takeguchi whose telephone number is (703) 305-8115. The examiner can normally be reached on Monday - Friday, 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

KT
Kathy Takeguchi
Art Unit 2187
July 8, 2003

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100